forming a contact hole in said first insulating layer and said second insulating film located between said first and second wirings, wherein said contact hole is defined by said line/space pattern and said first and second wirings.

131. A method of manufacturing a semiconductor device comprising the steps of:

forming first and second conductive films at a predetermined interval on a first insulating film;

forming a second insulating film on said first conductive film;

forming a line/space pattern on said second insulating film, said line/space pattern being intersected perpendicularly to said first and second conductive films; and

forming a contact hole in said first and second insulating films located between said first and second conductive films, wherein said contact hole is defined by a line/space pattern and said first and second conductive films.

B1 cont

132. A method of manufacturing a semiconductor device comprising the steps of:

forming first and second conductive films at a predetermined interval on a first insulating film;

forming a second insulating film on said first conductive film;

forming a line/space pattern on said second insulating film, said line/space pattern being intersected perpendicularly to said first and second conductive films; and

forming a contact hole in said first and second insulating films by etching said first and second insulating films using said line/space pattern and said first and second conductive films as a mask.

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14~~33~~. A method of manufacturing a semiconductor device comprising the steps of:

forming a transistor on a surface of a semiconductor substrate, said transistor having a gate electrode and a source/drain region;

forming a first insulating film covering said transistor;

forming first and second contact holes in said first insulating film, said first contact hole exposing a first region of said source/drain region, said second contact hole exposing a second region of said source/drain region;

forming first and second conductive films in said first and second contact holes, respectively;

forming a second insulating film on said first insulating film;

forming a third contact hole in said second insulating film, said third contact hole exposing said first conductive film;

B1 cont

forming a third conductive film in said third contact hole;

forming a bit line on said second insulating film, said bit line including a fourth conductive film connected to said third conductive film and a third insulating film on said fourth conductive film, and said bit line being located so as to intersect perpendicularly to a word line connected to said gate electrode;

forming a fourth insulating film on said second insulating film;

forming a line/space pattern on said fourth insulating film which intersects perpendicularly to said bit line;

forming a fourth contact hole in said second insulating film using said line/space pattern and said bit line as a mask, said fourth contact hole exposing said second conductive film;

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forming a fifth conductive film in said fourth contact hole; and

forming a capacitor above said bit line, said capacitor being connected to said fifth conductive film.

34. A method of manufacturing a semiconductor device comprising the steps of:

forming an element separation insulating film in a semiconductor substrate for dividing an element region;

forming a transistor in said element region, said transistor having a gate insulating film, a gate electrode connected to a word line and a source/drain region;

forming a first insulating film, said first insulating film covering said element separation insulating film and said transistor;

forming a first contact hole in said first insulating film, said first contact hole reaching a first region of said source/drain region of said transistor;

forming a second contact hole in said first insulating film, said second contact hole reaching a second region of said source/drain region of said transistor;

forming a first conductive plug for filling up said fist contact hole;

forming a second conductive plug for filling up said second contact hole;

forming a second insulating film, said second insulating film covering said first insulating film and said first and second conductive plugs;

forming a bit line contact in said second insulating film, said bit line contact reaching said first conductive plug;

forming a bit line in said second insulating film and said bit line contact, a lower part of said bit line including a conductive film and an upper part including a third insulating film;

forming a fourth insulating film on said second insulating film and said bit line;

forming a contact hole for a storage node on a side of said bit line and through said fourth insulating film and said second insulating film, said contact hole reaching said second conductive plug;

forming a fifth insulating film at least on a side wall of said conductive film and a side wall of said second insulating film on said bit line exposed from said contact hole; and

forming a capacitor having a storage node, a plate electrode above said storage node and a capacitor insulating film formed therebetween, said storage node being electrically separated from said conductive film by said fifth insulating film and connected to said second conductive plug via said contact hole,

wherein said contact hole for said storage node is defined by a line/space pattern which intersects perpendicularly to said bit line.

35. The method according to claim 34, wherein said third insulating film is a silicon nitride film and said second and fourth insulating films are silicon oxide films.

36. The method according to claim 34, wherein said fifth insulating film is one of a silicon oxide film and a composite film of a silicon nitride film and a silicon oxide film, and has a smaller dielectric constant than a silicon nitride film.

37. A method of manufacturing a semiconductor device comprising the steps of:

forming an element separation insulating film on a semiconductor substrate for dividing element regions;

forming a plurality of transistors in said element regions, said transistors respectively having a gate insulating film, a gate electrode connected to a word line and a source/drain region;

forming a first insulating film, said first insulating film covering said element separation insulating film and said transistors;

forming first contact holes in said first insulating film, said first contact holes reaching first regions of said source/drain regions of said transistors;

forming second contact holes in said first insulating film, said second contact holes reaching second regions of said source/drain regions of said transistors;

forming a first conductive plug for filling up said respective first contact holes;

B1 cont

forming a second conductive plug for filling up said respective second contact holes;

forming a second conductive plug for filling up said respective second contact holes;

forming a second insulating film, said second insulating film covering said first insulating film and said first and second conductive plugs;

forming a bit line contact in said second insulating film, said bit line contact reaching said respective first conductive plugs;

forming bit lines respectively on said second insulating film and said bit line contact, a lower part of said bit lines including a conductive film and an upper part including said third insulating film;

forming a fourth insulating film on said second insulating film and said bit line;

forming a contact hole for a storage node between said bit lines and through said fourth insulating film and said second insulating film, said contact hole reaching said second conductive plug;

forming a fifth insulating film at least on a side wall of said conductive film and a side wall of said second insulating film on said bit line exposed from said contact hole; and

forming a capacitor, said capacitor having a storage node, a plate electrode above said storage node and a capacitor insulating film formed therebetween, said storage node being electrically separated from said conductive film by said fifth insulating film and connected to said second conductive plug via said contact hole,

B1 cont'd

wherein said contact hole for said storage node is defined by a line/space pattern which intersects perpendicularly to said bit line.

19 ~~38~~. The method according to claim ~~37~~ 18, wherein said third insulating film is a silicon nitride film, and said second and fourth insulating films are silicon oxide films.

20 ~~39~~. The method according to claim ~~38~~ 19, wherein said fifth insulating film is one of a silicon oxide film and a composite film of a silicon nitride film and a silicon oxide film, and has a smaller dielectric constant than a silicon nitride film.--